Low-Loss High-Isolation 60-80 GHz GaAs SPST PIN Switch

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Abstract — **Low-loss high-isolation GaAs SPST PIN diode switch for millimeter wave applications is presented. Modeling of PIN diode switches using full-wave electromagnetic simulators by including the semiconductor properties of the diode mesa layers is explained. This approach eliminates the necessity of model extraction from measurements in most cases. In addition, usage of simulation tools allows the optimization of diode structure for minimum insertion loss. Main loss mechanisms of GaAs PIN diodes at mm-wave frequencies are explained. Measurement results of a newly developed CPW SPST 55-85 GHz GaAs PIN switch are presented and compared with simulations. The developed shunt switch has 0.6 dB insertion loss and 20 dB return loss in the off state (through) at 75 GHz. It has 20 dB insertion loss and 1 dB return loss in the on state (isolation) at the same frequency.**

I. INTRODUCTION

Millimeter-wave (mm-wave) GaAs PIN diode switches are extensively used in communication and radar systems. For instance, in High Resolution Radar (HRR) for automotive at 24 GHz, the demand for minimum and maximum radar ranges, which changes from 30 cm to 30 m, requires very high isolation and fast Tx/Rx switch. In another application, the design of Autonomous Cruise Control (ACC) radars for automotive at 77 GHz requires very low-loss and high frequency switch to form the transmit pulse. In all of the examples given above, GaAs PIN diodes are commonly used in designing the low-loss switch circuits. Since the mm-wave energy is difficult and expensive to generate, switch losses become a paramount consideration and should be minimized as much as possible. In this paper, we will present a very low-loss high-isolation CPW GaAs SPST PIN diode switch manufactured in the M/A-COM's GaAs foundry. A novel way of PIN diode modeling using full-wave electromagnetic (EM) simulators will be also explained.

W-band and Ka-band PIN switches have been previously reported by other authors [1-3]. Although the isolation reported in [1] is good (25 dB @ 83 GHz), the insertion loss was high (1.3 dB @ 83 GHz). On the other hand, the insertion loss reported in [2] is excellent (0.5 dB @ 80 GHz), but the isolation was relatively poor (11 dB @ 80 GHz). The 60-80 GHz SPST PIN diode switch reported in this paper has both low-insertion loss and high-isolation (0.6 dB and 20 dB, respectively, @ 75 GHz).

II. DESIGN OF THE SPST SHUNT PIN SWITCH

Single-pole single-throw (SPST) switches are the basic building blocks of higher order switch configurations. There are different ways of implementing SPST switches. Shunt configurations are usually used at high frequencies for their high-power handling capability and low insertion loss. The disadvantage of shunt configuration is that it needs $\lambda/4$ long transmission lines before diodes for SPDT (or higher order) switches. Because it does not need $\lambda/4$ transmission lines, series configuration may provide more compact designs but with increased insertion loss. To design a low-loss high-isolation shunt PIN switch, it is necessary to reduce the series resistance of the diode and tune out the off-state capacitance with a proper matching network. Reducing the series resistance provides a low-resistivity path to the ground when the shunt diode is turned on, hence the high isolation. When the diode is turned off, it presents an off-state capacitance, which should be tuned out to maximize the return loss hence reducing the insertion loss. The latter one can be conveniently achieved by adjusting the length of the air-bridges that connect anode of the diode to microstrip line. Consequently, by proper selection of the diode radius, semiconductor properties, and air-bridge dimensions, low-loss high-isolation shunt diodes can be designed. In this paper, we employ CPW configuration because it minimizes the ground inductance which helps to increase the isolation. Fig. 1 shows the mesa structure of the GaAs PIN diode.

Contact (R_c) and spreading resistances (R_s) are the two important phenomena that must further be discussed in detail. Especially in a CPW configuration or in a series diode, the current that flows through the forward biased diode into the diode N+ layer spreads sidewise towards the N-ohmic (see Fig. 1) which is called as "spreading resistance." This mechanism causes losses due to the conductivity of the N+ layer. Therefore, it is desirable to minimize these losses by increasing the doping of the N+ layer and/or optimizing the geometry for a minimum resistance. Contact resistance occurs when a semiconductor material is made contact with a metal. Due to the properties of this contact, the average path of the current through the N+ layer to the N-ohmic is increased. To quantify the contact resistance, usually a length is given in which the transverse distance traveled by the current

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exceeds this length by approximately 3 times then it is assumed that the current is completely transferred to the contact material. These two resistances are important and can be a significant contributor to the total loss of the diode in mm-wave frequencies. Although the full-wave simulation automatically takes into account the spreading resistance, contact resistance is relatively difficult to simulate. This is because it requires an addition of a very thin contact layer with appropriate conductivity between the N-ohmic and N+ layer. During the design of the switch, N-layer was kept as wide as possible to reduce the spreading resistance.

III. PIN DIODE MODELING USING EM SIMULATORS

The established way of modeling PIN diodes is through either semiconductor simulations or experimental data, which is preferably obtained from design of experiments (DOE) although straight measurement results could also be used. The semiconductor simulations provide the intrinsic parameters of the diode junction, which is insufficient to be directly used in high-frequency designs because it does not give the parasitic effects, such as air-bridge inductances, capacitances between the air-bridges and N-Ohmic layer, and spreading resistance due to N-Ohmic layer. Therefore, the designer usually separately simulates the metalizations around the diode structure using full-wave EM simulators as a multiport circuit and then replaces the intrinsic model of the PIN diode at the appropriate position in the circuit. Although this approach seems reasonably accurate, it has the problem of proper placement of the intrinsic diode in the circuit since the placement of the intrinsic diode model requires usage of some sort of internal ports in the EM simulator, which modifies the original structure and is not accurate. Measurements, on the other hand, provide the utmost characterization of the PIN diode. Nevertheless, measurements do not easily allow optimization of diode structure and iteration period is longer.

The novel modeling approach that is going to be demonstrated in this paper is based on simulating the whole diode structure in EM simulator by assigning proper material constants to the semiconductor mesa layers used in the PIN diode. Note that since it is only required to have two different modes of operation in a PIN diode switch (on- and off-state), it is not required to model the actual semiconductor physics during simulations. Therefore, EM simulators are sufficient to model the PIN diodes with relatively good accuracy as long as the material properties (conductivity, dielectric constant, and dielectric loss) are known for given bias states. The advantage of this approach is the elimination of the two-step process of obtaining the diode model from semiconductor simulation (or measurements) and then using it as sub-circuit of a multiport EM simulation as explained above. This method will not only increase the accuracy because the structure is simulated as a whole, it will also enable optimization of diode structure for various parameters more easily. For instance, matching of the shunt PIN diode off-state capacitance with air-bridge inductances can be very accurately done through this method. Another example is the optimization of diode area for minimum spreading resistance.

To simulate the PIN diode through the full-wave electromagnetic simulators, we have to determine material properties of the intrinsic PIN diode first. The intrinsic resistance of the PIN diode under forward bias can be calculated using the following expression [4,5]:

$$R_i = \frac{1}{I_F \tau} \frac{w_i^2}{4} \frac{\mu_n + \mu_p}{\mu_n \mu_p} \tag{1}$$

where w_i is the thickness of the intrinsic region, μ_p is the mobility of holes, μ_n is the mobility of electrons, I_F is the forward bias DC current and τ is the effective carrier lifetime in the intrinsic region. In our case, μ_p and μ_n are 400 cm^2/Vs and 8000 cm^2/Vs, respectively. Note that these mobilites are given for the I-region. As one can see, this expression is independent of the area of the I-region. The reason is that the conductance of the I-region in forward bias is determined by the carriers injected through constant bias current I_F. No matter what the area is, this forced current dictates the conductance, which can be calculated from (1) as follows:

$$\sigma = \frac{1}{R_i \frac{A}{w_i}} = 4 I_F \tau \frac{\frac{\mu_n \mu_p}{\mu_n + \mu_p}}{w_i A} \tag{2}$$

where A is the area of the depletion region. Hence, when modeling the diode under forward bias condition, one must enter the conductance in parametric form to the EM simulator using (2) as a function of area and thickness of the I-region. The constant depletion capacitance presented by the junction at reverse bias is given for GaAs by the following expression:

$$C_i = \varepsilon \frac{A}{w_i} \tag{3}$$

where ε is the dielectric constant of the depletion layer material ($12.9 \times 8.854 \times 10^{-12}$ F/m for GaAs). In our case, w_i and R (average radius of the I-region) are 2.0 μm and 26 μm, respectively. This gives an approximate junction capacitance of 30 fF. In GaAs, almost the entire I-region is swept-off when the junction is reverse biased. Hence, when modeling the diode under reverse bias condition, it is

practically sufficient to model the I-region as a parallel plate capacitor by entering the appropriate dielectric constant to the EM simulator for the I-region.

An alternative graphical method can also be used to determine the conductivity of the I-region instead of using (2) as follows: Suppose that the DC resistivity of sample PIN diodes with various radii are determined experimentally and plotted as a function of the inverse current. Since from (1) we know that the intrinsic impedance of the I-region goes to zero when the current approaches infinity, simple linear extrapolation of the data points can provide us the overall contact and intrinsic resistance values as shown in Fig. 4. The resistance values read at the points where the lines are crossing vertical axis are the contact resistances (R_c). After determining the contact resistance for a particular diode, the intrinsic resistance (R_i) can be determined by subtracting the contact resistance from the resistance value corresponding to a given DC current. Then, conductivity of the I-region can be easily calculated. Note that the contact resistance value obtained from the single via-hole case is the most accurate representation of the contact resistance because the spreading resistance is minimum. This is because the ground via-hole is placed directly beneath the diode in the single via-hole configuration. However, for the double via-hole configuration, where the via-holes are placed on the sides, the spreading resistance becomes important because the current needs to travel the N-ohmic interface transversely to reach the side via-holes.

As a conclusion, it is sufficient to represent the intrinsic region with a lossless dielectric in the reverse bias condition because, in a GaAs PIN diode, almost all of the carriers are swept from the intrinsic region in the reverse bias. In the forward bias, on the other hand, the intrinsic region must be replaced with a lossy dielectric whose conductivity is assigned properly. The N+ and P+ regions are represented by dielectrics whose conductivities are determined from the respective carrier mobility and concentration. Fig. 2 summarizes the properties of the mesa layers that will be used in the simulations. Fig. 3 shows the full-wave EM simulator model.

IV. RESULTS

Measurement results of the low-loss high-isolation SPST GaAs PIN switch are shown in Fig. 5 through Fig. 8 and compared with the simulation results obtained from Ansoft HFSS and CST Microwave Studio. The results shown are on-wafer measurements taken using HP 8510C VNA. The calibration method employed is the Multiline method by NIST, which is the most accurate on-wafer calibration technique for mm-wave frequencies to author's knowledge. This is because the launcher parasitics are automatically extracted during the Multiline calibration.

In the reverse bias case (0 V), the most important parameter is the insertion loss for a shunt switch. The measured insertion loss is less than 0.6 dB between 55 and 75 GHz. In addition, it can be seen that the difference between simulations and measurements is around 1/10th of a dB. In the forward bias (10 mA), the insertion loss determines the isolation for a shunt switch. The measured insertion loss in this case is greater than 20 dB between 55 and 75 GHz. Note that there is a resonance behavior observed around 80 GHz in the measurements for the forward bias case, which is probably due to the finite ground plane configuration of the CPW structure.

For the PIN diode developed in this work, R_i=0.6 Ohm, R_c=1.6 Ohm, and C_i=30 fF. An important figure of merit of PIN diodes is the cut-off frequency, which is defined as follows [5]:

$$f_c = \frac{1}{2\pi\sqrt{R_{ON}\cdot R_{OFF}}C_{OFF}} \qquad (4)$$

where R_{ON}=1.6+0.6 Ohm, R_{OFF}=1.6 Ohm, and C_{OFF}=30 fF, which gives f_c as 2.8 THz.

V. CONCLUSION

We presented low-loss high-isolation GaAs SPST PIN diode switch for millimeter wave applications. The modeling method is based on complete simulation of the switch structure including the diode semiconductor mesa layers at specified bias conditions. The semiconductor layers are replaced with appropriate lossy dielectrics whose parameters are determined based on the bias condition. The modeling procedure can accurately predict spreading resistance, intrinsic resistance, and all parasitic effects, which are important in high frequencies.

ACKNOWLEDGEMENT

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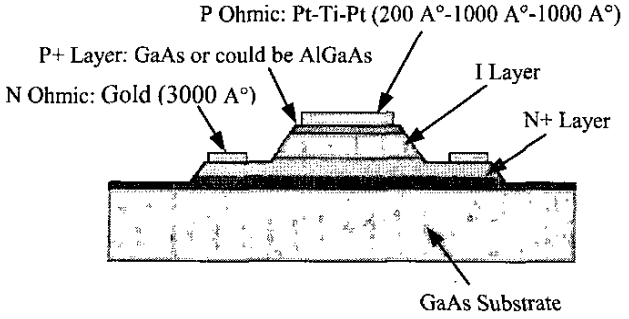

Figure 1: Basic mesa structure of the mm-wave GaAs PIN diode.

	N+ Layer	P+ Layer	I Layer	
Thickness	1.5 μm	0.5 μm	2.0 μm	
Relative dielectric constant	12.9	12.9	12.9	
Dielectric loss tangent	~0	~0	0.006	
Conductivity	100000 S/m	38462 S/m	*On*	5416 S/m
			Off	~0 S/m

Figure 2: Properties of the semiconductor layers of the GaAs PIN diode for electromagnetic simulations.

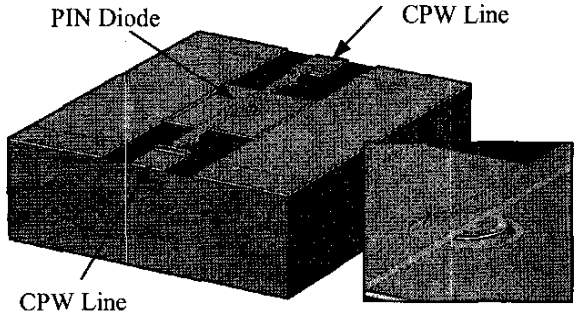

Figure 3: CST Microwave Studio model of the shunt SPST GaAs PIN diode switch. The N-Ohmic is 100 μm x 100 μm and the top diameter of P+ is 24 μm. The air-bridge is 10 μm wide.

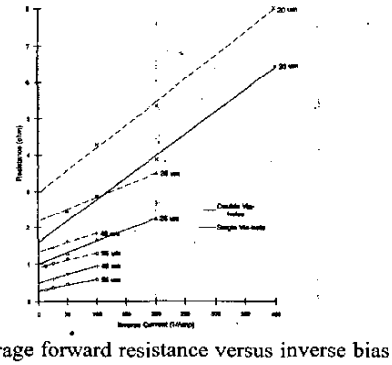

Figure 4: Average forward resistance versus inverse bias current for single- and double-via microstrip SPST PIN switches for different anode diameter.

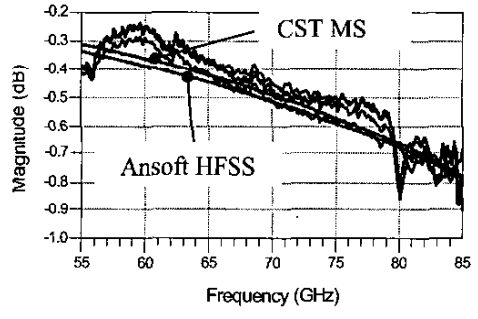

Figure 5: Measured and simulated insertion loss (S_{21}) of the shunt SPST switch under reverse bias condition.

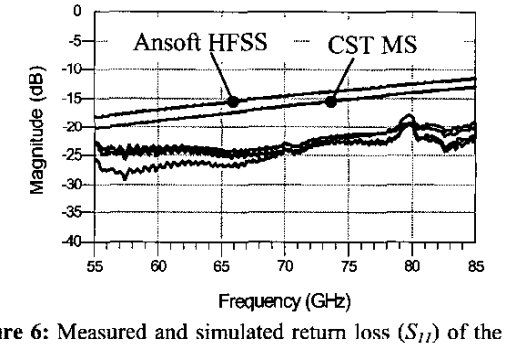

Figure 6: Measured and simulated return loss (S_{11}) of the shunt SPST switch under reverse bias condition.

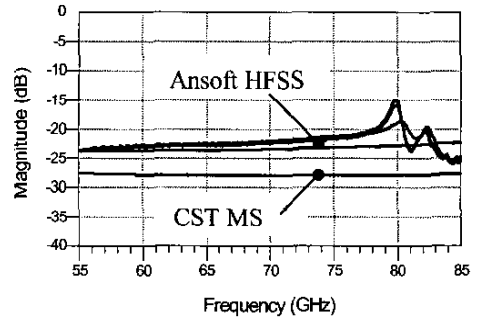

Figure 7: Measured and simulated insertion loss (S_{21}) of the shunt SPST switch under forward bias condition.

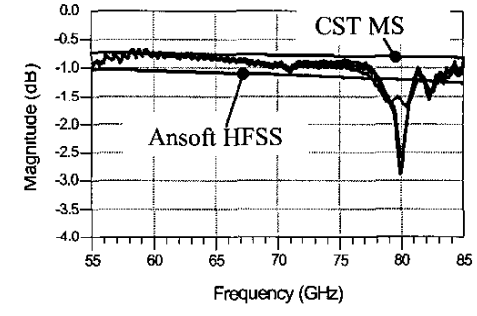

Figure 8: Measured and simulated return loss (S_{11}) of the shunt SPST switch under forward bias condition.